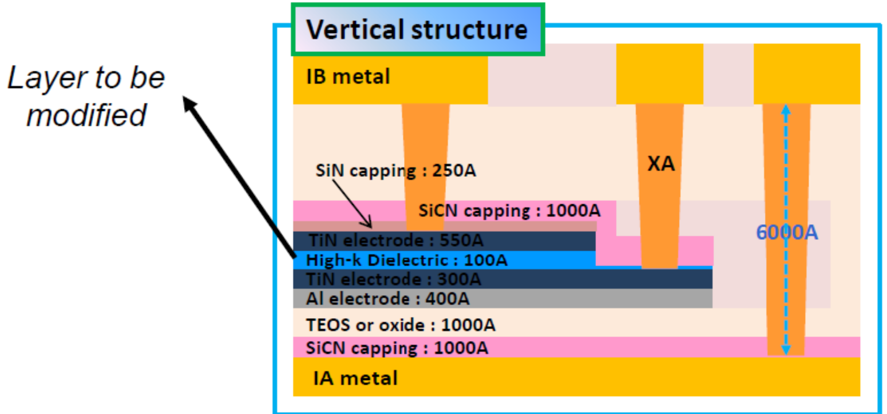
PCN 11773 – Additional information

MIM module process change in Samsung Foundry: MIM HAH stack implementation on 32LP, 28LP and 28FD Technologies

WHAT is the change?

Metal Insulator Metal (MIM) capacitance insulator (dielectric) change from Ta2O5 material to HfO2/Al2O3/HfO2 (HAH) tri-layer for performance and throughput/capacity improvement



CONDUCTORS AND DIELECTRICS				
Layers (for MIM)	Parameters	Thick	Thick Var	K
Units	Units	[A]	[A]	
Above MIM top plate (conformal)	Nitride	600	60	8.1
MIM top plate	TiN	550	55	
Dielectric between MIM plates	MIM diel	115	11	25
MIM bottom plate	TiN	300	45	
MIM bottom plate	Al	400	40	
Below MIM bottom plate	Oxide	1000	100	4.2

Process items	Current process	Current tool	New process	New tool
MIM Insulator (dielectric) Deposition	Ta_2O_5 layer	Emeral3000	$HfO_2/Al_2O_3/HfO_2$ (HAH) tri-layer	Pulsar

WHY?

Samsung Foundry decided to qualify a new equipment on Line 32LP, 28LP and 28FD for performance and throughput/capacity improvement:

- Ta2O5(TAO) deposition tool out of production (only 3 chambers worldwide)
- Complex PM and parts delivery time higher for TAO
- Higher support on HAH stack, because used on advanced technology nodes (14/10nm)

❶ Chamber comparison

	TAO (POR)	HAH (SF Proposal)
Model	Emeral3000	Pulsar
Status	Out of production (3 chambers world wide)	Production (many)
Chamber view	Insulator, Gas Line, PVM, Gas Plate	Chamber, Gas Line, Distribution, susceptor
비 고	**Complex** 43ea PM Parts Total 150ea Parts	**Simple** 15ea PM Parts Total 37ea Parts

WHEN will this change occur?

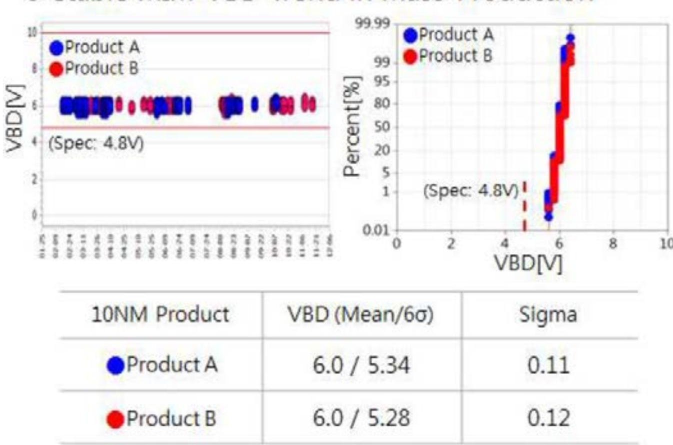
New process plan to be implement in Fab on W1945
Foundry plan to remove Old tool on W1950

HOW will the change be qualified?

Wafer Level Qualification:

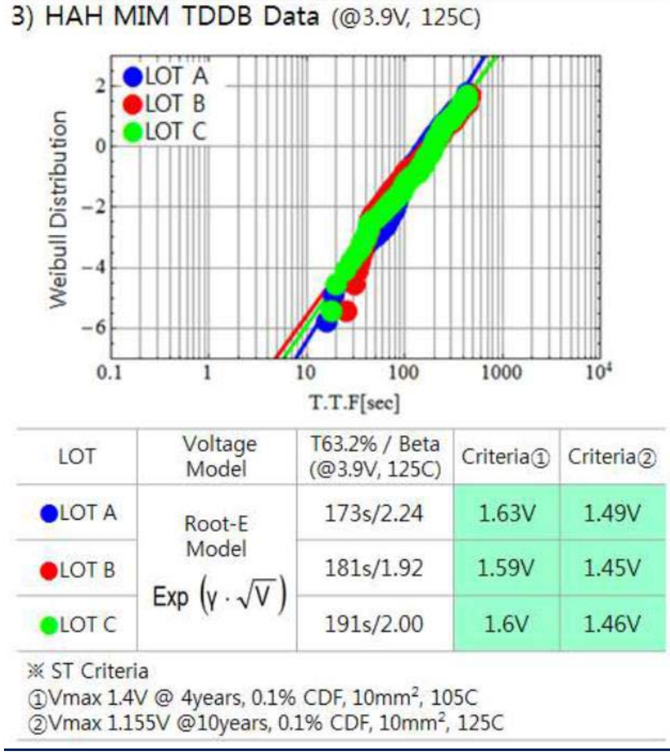
MIM capacitor with new process has been qualified through wafer level reliability test

- Extrinsic Breakdown (Vramp): No extrinsic breakdown found in other product Mass production



10NM Product	VBD (Mean/6σ)	Sigma
Product A	6.0 / 5.34	0.11
Product B	6.0 / 5.28	0.12

- Breakdown Life time Model (TDDB) on 3 lots: Passing Mission Profile criteria (Vmax > Vuse)



LOT	Voltage Model	T63.2% / Beta (@3.9V, 125C)	Criteria①	Criteria②
LOT A	Root-E Model $Exp(\gamma \cdot \sqrt{V})$	173s/2.24	1.63V	1.49V
LOT B		181s/1.92	1.59V	1.45V
LOT C		191s/2.00	1.6V	1.46V

※ ST Criteria
①Vmax 1.4V @ 4years, 0.1% CDF, $10mm^2$, 105C
②Vmax 1.155V @10years, 0.1% CDF, $10mm^2$, 125C

Product Qualification:

See Appendices for Qualification plan.
Estimate Date of Final Qualification: W1945

APPENDICES:

APPENDIX 1 Qualification plan

APPENDIX 1: QUALIFICATION PLAN

Reliability Qualification Plan:
MIM module process change in Samsung Foundry:
MIM HAH stack implementation on 32LP, 28LP and 28FD Technologies

General Information	
Silicon process technology	*CMOS28nm LP*
Affected products	*H310 (Cannes 2.0)*

Locations	
Wafer fab location	*Samsung Foundry*

Objectives:

The objective of this qualification plan is to define the trials to validate the Metal Insulator Metal (MIM) capacitance insulator (dielectric) change from Ta2O5 material to HfO2/Al2O3/HfO2 (HAH) tri-layer for performance and throughput/capacity improvement at Samsung Foundry on 32LP, 28LP and 28FD Technologies

Estimate Date of Final Qualification: W1945

Description of the change:

Process items	Current process	Current tool	New process	New tool
MIM Insulator (dielectric) Deposition	Ta_2O_5 layer	Emeral3000	$HfO_2/Al_2O_3/HfO_2$ (HAH) tri-layer	Pulsar

Strategy for qualification:

Focus on two Test Vehicles products worst case in term of MIM area and MIM voltage Vuse.

Product	Comments
Product A	MIM area: 3.77mm2 @ 1.0V MIM area: 19.92mm2 @ 1.1V
Product B	MIM area: 52.5 mm2 @ 0.70 V
H310	MIM area: 5.6 mm2 @ 1.0V

Lot definition and traceability:

Lot Nb	Product	Si Foundry
1	Product A	Samsung
2	Product A	Samsung
3	Product B	Samsung

Reliability Test Results:

Test	Test short description					
	Method	Conditions	SS/Lot	Lot n#	Duration	
3 IR	Reflow simulation (3 times) with standard JEDEC profile					
	JESD22-A113		120 120 60	1 2 3	NA	
3 IR+TC	Temperature cycling test					
	JESD22-A104	Ta= -55/+125°C for Product A Ta= -40°C/125°C for Product B Steps: 0, 500, 1000 cycles	30 30 30	1 2 3	1000 cy	
3 IR+HTOL	High Temperature Operating Life test					
	JESD22-A108	Vnom + 10% Tj>135°C Steps: 0, 500, 1000 hours	80 80 30	1 2 3	1000 hrs	

Comment about Lot 3: Due to high device costs and board availability, only 30 samples used for HTOL trial.

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